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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/799,877	03/15/2004	Si-Bum Kim	123037-05005048	8351

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EXAMINER	
TRINH, MICHAEL MANH	
ART UNIT	**PAPER NUMBER**
2822	

DATE MAILED: 12/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/799,877	KIM, SI-BUM	
	Examiner	Art Unit	
	Michael Trinh	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *16-18* is/are allowed.

6)☒ Claim(s) *1,2 and 4-15* is/are rejected.

7)☒ Claim(s) *3* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/15/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

*** This office action is in response to filling of the application on March 15, 2004. Claims 1-18 are pending.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

3. Claims 1-2,4-6,8-10,15 are rejected under 35 U.S.C. 102(e) as being anticipated by Thomas (2003/0234416).

Re claim 1, Thomas teaches a method for forming a semiconductor device comprising at least the steps of: a) forming an insulation layer 18 in a capacitor region and a metal interconnection region on a substrate 17 (Fig 1; paragraph 15); b) forming a metal interconnection 16 in the metal interconnection region of the insulation layer 18 by performing a dual damascene process (paragraphs 16-18); and c) forming a capacitor in the capacitor region of the insulation layer such that the capacitor is in a same level as the metal interconnection in the insulation layer (Figs 3-5; paragraphs 22-27). Re claim 2, wherein the step c) includes : forming a first trench (Fig 1; paragraph 16-19) at the capacitor region of the insulation layer 18; forming a first metal interconnection 16 inside the first trench; forming a second trench 22 (Fig 2; paragraphs 20-22) by removing the insulation layer 18 between the first metal interconnection; and forming a capacitor composed of a first electrode 26, a dielectric layer 30 and a second electrode 27 on side and bottom surfaces of the second trench 22 (Figs 3-5; paragraphs 23-27). Re claim 4, further forming a second metal interconnection 33/16/28 connected to the second electrode of the capacitor (Fig 6). Re claim 5, wherein the first metal interconnection 16 includes copper (paragraph 17). Re claim 6, wherein the first and second electrodes 26,27 includes tungsten (W) (paragraph 23). Re claim 8, Thomas teaches a method

for forming a semiconductor device comprising at least the steps of: a) forming an insulation layer including a first insulation layer (level 14; Fig 1) and a second insulation layer (level 13) in a capacitor region and a metal interconnection region on a substrate 17 formed with a lower conductive layer 16 at level 12 (Fig 1; paragraph 15); b) forming an interconnection trench in the metal interconnection region, a first trench in the capacitor region, and a via hole connected to the lower conductive layer by selectively etching the insulation layer (Fig 1); c) forming a copper interconnection, a firs copper interconnection and a via contact plug by forming a first copper layer in the interconnection trench, the via hole and the first trench and planarizing the resulting structure (Fig 1; paragraphs 15-19); forming a second trench 22 by selectively etching the second insulation layer 18 (Fig 2 at level 13) in the capacitor region (Fig 2; paragraphs 20-22); forming a capacitor composed of a first electrode 26, a dielectric layer 30 and a second electrode 27 on side and bottom surfaces of the second trench 22 (Figs 3-5; paragraphs 23-27); and forming a second copper interconnection by forming a second copper layer on the capacitor and planarizing the second copper layer (Figs 3-5; paragraphs 22-27). Re claims 9-10, wherein an etching blocking layer 19,20 and as a hard mark is formed between and on the first and second insulating layers 18 (Fig 1, paragraph 18). Re claim 15, wherein a first barrier metal and a second barrier metal 33 before forming the first and second copper 16 (Figs 1-4; paragraphs 17,19-26) .

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later

invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

3. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Thomas (2003/0234416) taken with Lur et al (5,449,630).

Thomas teaches a method for forming a semiconductor device as applied above to claims 1-2,3-6,8-10,15.

Thomas teaches (at paragraph 24) forming the dielectric comprising silicon nitride, but lacks mentioning of metal oxide dielectric as recited in claim 7.

However, Lur teaches (col 5, lines 10-21) employing a dielectric material including silicon nitride, tantalum oxide, strontium titanate, barium titanate, etc

It would have been obvious to one of ordinary skill in the art at the time the invention was made to the dielectric of Thomas by using tantalum oxide, strontium titanate, barium titanate, as taught by Lur. This is because of the desirability to form a dielectric having high-k dielectric constant in forming the capacitor.

4. Claim 11-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Thomas (2003/0234416) taken with Park et al (6,596,581).

Thomas teaches a method for forming a semiconductor device as applied above to claims 1-2,3-6,8-10,15.

Thomas lacks detailing about forming the interconnection trench and via holes (claims 11-12) and copper deposition techniques (claims 13-14).

However, re claims 11-12, Park teaches (at col 5, lines 10-21) forming the via hole either before or after forming interconnection trench and first trench; and re claims 13-14, forming a seed layer before electroplating a copper thereon (col 5, lines 50-67; col 6, lines 45-56; col 7, line 50 through col 8; Fig 8).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the trench and via holes of Thomas by forming the via hole either before or

after forming interconnection trench and first trench, and forming a seed layer before electroplating a copper thereon, as taught by Park. This is because these processes are alternative for substitution in forming the trench and via holes, wherein forming a seeding layer before copper electroplating deposition would enhance the copper deposition more reliable and uniform in the via holes, and enhance adhesion.

Allowable Subject Matter

5. Claims 16-18 are allowed.

6. Claim 3 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is a statement of reasons for the indication of allowable subject matter:

The references of record, alone or in combination, do not fairly anticipatively disclose each and every aspect of the claimed method, or fairly make a prima facie obvious case of the claimed method, in combination with other processing claimed limitations as recited in claims 16-18, which method as of claim 16 comprises a) forming an insulation layer including a first insulation layer and a second insulation layer in a metal interconnection region and a capacitor region on a substrate formed with a lower conductive layer; b) forming an interconnection trench in the metal interconnection region, a first trench in the capacitor region and a via hole by selectively etching the insulation layer; c) forming a copper interconnection, a via contact plug and a first copper interconnection by forming a first barrier metal and a first copper layer in the interconnection trench, the via hole and the first trench and planarizing a resulting structure; d) forming a second trench by selectively etching the second insulation layer around the first copper interconnection in the capacitor region; e) forming a third trench in the first barrier metal by selectively etching the first copper interconnection; f) forming a capacitor composed of a first electrode, a dielectric layer and a second electrode on side and bottom surfaces of the second and third trenches; and g) forming a second copper interconnection by forming a second copper layer on the capacitor and planarizing said second copper layer.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (571) 272-1847. The examiner can normally be reached on M-F: 8:30 Am to 5:00 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The fax phone number is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the receptionist whose telephone number is (703) 308-0956.

Oacs-18

Michael Trinh
Primary Examiner